A New Large-Signal AlGaAs/GaAs HBT Model Including Self-Heating Effects, with Corresponding Parameter-Extraction Procedure

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Abstract— **Accurate modelling of the microwave large-signal characteristics of AlGaAs/GaAs Heterojunction Bipolar Transistors (HBT's) is extremely useful for microwave power applications of the device. This paper presents a new type of HBT large-signal model which is valid for dc, small-signal and large-signal ac modes of operation. The model may be used over a wide range of operating conditions and includes allowance for self-heating effects which are very important for HBT's. Through the use of several novel features, the proposed approach is differentiated from the traditional Ebers-Moll or Gummel-Poon BJT representations. The new model is accompanied by a very simple parameter extraction process requiring only a series of conventional dc and multi-bias point small-signal S-parameter measurements. Finally, the model is validated by independent power sweep measurements on HBT's from two different manufacturers.**

I. Introduction

HETEROJUNCTION bipolar transistors (HBT's), based either on the material system AlGaAs/GaAs or GaInP/GaAs, are widely used in many analog and digital applications [1], [2], [10], and [27]. For modern CAD-based circuit design, there is a need for a unified HBT circuit model which should be valid for dc, microwave small-signal and large-signal operation. The main purpose of this paper is to introduce and describe a large-signal AlGaAs/GaAs HBT model.

Although the HBT is a relatively new type of device, there are no fundamental differences in its basic operating principles compared to the normal homojunction bipolar transistor (BJT). On this basis, many designers have directly used conventional BJT models such as the Ebers-Moll or Gummel-Poon for circuit designs incorporating the HBT [3]–[7]. Nevertheless, the models which result are usually only useful in restrictive areas of application because HBT's exhibit several significant differences in electrical performance compared to Si BJT's, which cannot be adequately represented by traditional BJT models. Many existing HBT-specific models are only valid for dc or small-signal ac. Some of them can be extended into nonlinear operation by using Volterra series for simulation at medium input signal level and at a fixed bias point. Grossman and Choma [6] have presented an Ebers-Moll type large-signal HBT model which includes many high-order effects to achieve accuracy. Their model is rather complex for use in commercial software environments, and many of the associated parameters are obtained through semiconductor/physical analysis and might be difficult to extract without a detailed knowledge of the device fabrication process.

Until the time of writing, it is believed that no unified HBT model has been reported which can simultaneously cover dc, small-signal AC and microwave large-signal applications. This paper presents such a model, which is quite different from conventional Ebers-Moll or Gummel-Poon models, and is best described as a semi-experimental based model, valid for the entire application region from dc to large-signal microwave conditions. The main distinctive features of this model are: 1) an alternative basic topology is proposed, involving a division of the base region into several sub-nodes; 2) two temperature-dependent diodes are used and then incorporated within a new *temperature-sensitivity partitioning technique* to simulate self-heating effects; 3) two different experimental ideality factors are used for the above two diodes and also two non-linear resistors to simulate non-uniform gain; 4) a new method is introduced to re-construct the total mobile charge related to the collector current; and 5) the proposed model also yields a very simple, direct and reliable parameter extraction process.

In Section II, the motivation for developing a new large-signal HBT model is discussed. In Section III, the new large-signal HBT model is presented, and the physical meaning of the model parameters is discussed. Section IV provides a detailed discussion of the proposed method to incorporate self-heating effects into general-purpose circuit simulators. Section V introduces the associated systematic parameter extraction procedure, and, finally, Section VI gives several examples of experimental large-signal verification of the model.

II. Motivation for Developing a New HBT Model

Since the HBT and BJT have similar operating principles, the reasons to develop a new model rather than to use a conventional BJT model must be clarified. The typical dc characteristics of a (high-frequency) Si BJT are shown in Fig. 1(a) and (b). Fig. 1(a) is a Gummel plot which is measured with $V_{bc} = 0$ and shows a plot of $\log(I_c)$ and $\log(I_b)$ against V_{be}. Several distinct regions can be identified

Manuscript received July 29, 1994; revised December 14, 1994. This work was supported by ESPRIT 6050 MANPOWER and Forbairt (the Irish National Science and Technology Research Agency).

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IEEE Log Number 9412054.

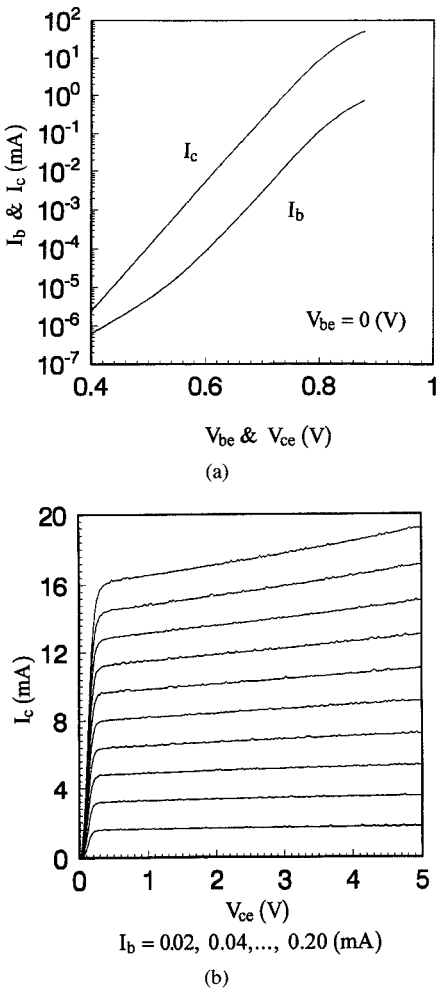

Fig. 1. DC measurement results of a NE85637 microwave silicon homojunction BJT: (a) log (I_b) and log (I_c) versus V_{be} (Gummel plot); (b) I_c versus V_{ce} at different fixed I_b values (output characteristics).

on this plot. In the low-current region, the base current is dominated by recombination current components, both at the surface and in the emitter-base *space-charge region* (SCR). Normally in this region the ideality factor of I_b (nonideal base-emitter emission coefficient in SPICE) lies between 1 and 2, which is larger than the ideality factor of I_c, and as a result, the dc current gain increases with increasing V_{be} [8], [9]. In the mid-current region, the base current is dominated by recombination current components in the neutral base region, and the ideality factor of I_b in this region is approximately the same as the ideality factor of I_c. Hence, the $\log(I_c)$ and $\log(I_b)$ curves for the mid-current region are two parallel straight lines and the BJT exhibits constant current gain behavior over several decades of current. In the high current region, $\log(I_c)$ and $\log(I_b)$ deviate from a straight line due to voltage drops across the emitter and base resistances, and also due to the Webster Effect (also called the conductivity modulation effect) [8]. Fig. 1(b) shows the usual common emitter output characteristics for a BJT, in which it may be observed that I_c increases as V_{ce} increases with constant I_b. This is the Early effect (or base width modulation) [8], [15], [25].

Based on this behavior, a normal BJT can be described using standard models derived from physical analysis, and some parameters of the model can be extracted from such measurement results. In the SPICE BJT model, two constants β_{FM} and β_{RM} are used to combine base and collector current together to produce the current gain [8], [9]. A normalized charge component q_b is used to modify the BJT characteristics in order to simulate the Webster Effect and the Early Effect. This SPICE model arises from application of the charge control concept [15].

Now consider Fig. 2(a) and 2(b), which show a typical set of AlGaAs/GaAs HBT dc characteristics. Comparing Fig. 1(a) with Fig. 2(a), several important differences are apparent in the latter case. In the low-current region, I_c and I_b are now dominated by leakage current (i.e. essentially ohmic behavior). In the mid-current region, the curves for $\log(I_c)$ and $\log(I_b)$ are two straight lines but no longer parallel and in fact, generally have quite different slopes. From a semiconductor point of view, this is due to the fact that the base current is dominated by several recombination current components over the entire forward active region in the case of the HBT. These components are the recombination current in the emitter-base SCR, recombination current at the emitter-base heterointerface, recombination current at the emitter-base SCR edge and recombination current in the neutral base region [11]. From a modelling point of view, therefore, the constant current gain region which covers most of the middle current region of a normal BJT, no longer exists in the case of the HBT.

For the high-current region, $\log(I_c)$ and $\log(I_b)$ start to deviate from linearity due to the effects of parasitic resistances. By observing Fig. 2(b), it is clear that the Early effect can be ignored. From a semiconductor point of view, this is because the high base doping of the HBT causes the Early voltage to be more than 100 V and generally negligible at room temperature [1], [6]. For the high-current region, I_c is observed to show a negative slope and the current gain therefore decreases with increasing V_{ce}. As mentioned earlier, this is due to strong self-heating effects when the power dissipation increases [6], [13], [16]. In the case of multi-finger power HBT's, for the region with very high collector current and collector-emitter voltage, the current gain can suddenly decrease by several orders of magnitude. This phenomenon is called gain collapse, and is attributed to a nonuniform temperature distribution across the emitter fingers [19].

Based on the above discussion, it is clear that neither the Ebers-Moll nor the Gummel-Poon model, which naturally predict constant current gain for most forward bias regions, are good candidates for most AlGaAs/GaAs HBT's, which instead exhibit non-uniform current gain for the same region. To resolve these modelling problems a new circuit model has been developed, as discussed in the next section.

III. The Proposed HBT Model

The most important requirement for a large-signal model is the ability to give correct predictions of current gain in the forward active region. To create a new model for the HBT which demonstrates this ability, we firstly assume that the relationship between the voltage across the BE heterojunction and I_b should follow the exponential function as a normal semiconductor junction does. It is also assumed that the

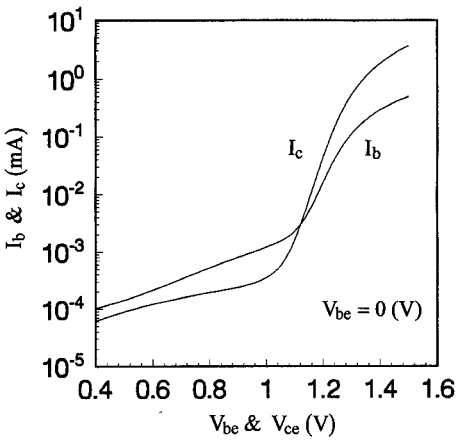

Fig. 2. DC measurement results of a typical AlGaAs/GaAs heterojunction bipolar transistor: (a) log (I_b) and log (I_c) versus V_{be} (Gummel plot); (b) I_c versus V_{ce} at different fixed values I_b (output characteristics).

Webster effect can be ignored for HBT's due to its high base doping level [6]. Based on these two assumptions, the new HBT model has been developed and is shown in Fig. 3(a).

A. Static Part of New HBT Model

The static part of the proposed model includes two temperature-dependent diodes and two nonlinear resistances, included so as to track accurately the dc characteristics of the HBT. To simulate the non-uniform current gain, the base region is split into several nodes, while two diodes with different characteristics simulate I_b and I_c independently. Of course this represents a considerable departure from conventional BJT modelling, but it does provide a new way to simulate non-uniform gain effects for the HBT. The equations for these two diodes are as follows:

For D_{be_ib}

$$I = I_{S\_ib}(T_j) \cdot (e^{V/(n_{be\_ib}(T_j) \cdot V_T(T_j))} - 1) \tag{1}$$

For D_{be_ic}

$$I = I_{s\_ic}(T_j) \cdot (e^{V/(n_{be\_ic}(T_j) \cdot V_T(T_j))} - 1) \tag{2}$$

where V and I are the voltage and current applied to the diode ports, n_{be_ib} and n_{be_ic} are the *experimental ideality factors* of these two diodes (the word *experimental* is used here to emphasise that this factor is more based on experimental results rather than a detailed physical analysis), $V_T(T_j)$ is the *thermal voltage* at T_j and T_j is explained below. Temperature-dependence in the diode characteristics is introduced by means of the following expressions for the saturation current and the experimental ideality factor [6], [8], [9], and [13]

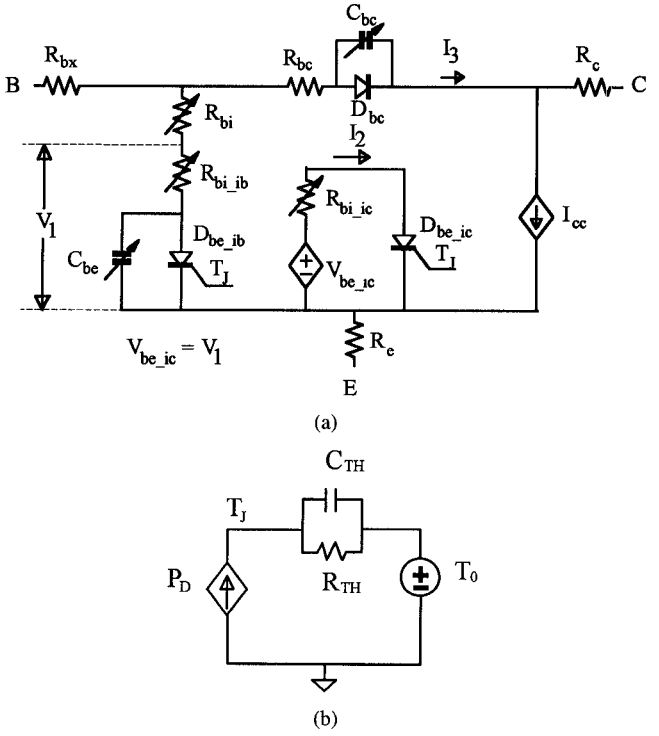

Fig. 3. (a) New large-signal HBT model. (b) Analogue thermal equivalent circuit used to calculate the junction temperature.

$$I_s(T_j) = I_s(T_0) \cdot e^{((1/T_0)-(1/T_j)) \cdot T_s} \tag{3}$$

$$n(T_j) = n(T_0) \cdot (1 + A_n \cdot \Delta T + B_n \cdot \Delta T^2) \tag{4}$$

where T_0 is ambient temperature, T_s is the saturation current temperature as defined by [6], A_n and B_n are two experimental coefficients, T_0 is 300 K, $\Delta T = T_j - T_0$ and T_j is the *computation junction temperature*. The latter term is used here as distinct from the real junction temperature, which might differ from T_j. The computation junction temperature is a tool to connect the dissipated power inside the HBT with the electrical behavior of the device. It is proportional to the weighted average temperature of the junction area, although that temperature distribution across the junction might have a complex spatial pattern. The computation junction temperature is calculated from the dissipated power inside the HBT by

$$P_D = I_B \cdot V_{BE} + I_C \cdot V_{CE} \tag{5}$$

$$P_D = \frac{\Delta T}{R_{TH}} + C_{TH} \cdot \frac{d(\Delta T)}{dt} \tag{6}$$

where R_{TH} is the *computation thermal resistance* and C_{TH} is the *computation thermal capacitance*. Again, these two terms are used to avoid confusion with the normal definitions of thermal resistance and capacitance. The equivalent circuit to describe (5) and (6) is shown in Fig. 3(b). It is worth indicating

that these equations are only a first-order approximation of the real thermal behavior of the HBT. The complete description of the thermal behavior is a very complex issue involving thermodynamic analysis. The electrical analogue equivalent of this description might be a multi-section RC network or RC transmission line. A detailed discussion of the self-heating effect and a method for its incorporation into commercial software packages, is provided in the next section.

The diode D_{bc} is used to simulate the BC homojunction of the HBT and it's temperature-dependence as shown in the following equation:

$$I = I_{s\_bc}(T_j) \cdot (e^{V/(n_{bc}(T_j)\cdot V_T(T_j))} - 1) \tag{7}$$

where the parameter definitions are the same as (1) and (2). In the interests of simplicity, since D_{bc} only affects the reverse operation region which is less important for most circuit designers, we normally do not include allowance for self-heating effects in this diode.

The two nonlinear resistances R_{bi} and R_{bi_ib} (or R_{bi_ic}) are used to adjust the high current region current gain and they can be approximated as suitable functions of the bias conditions. For the Siemens HBT #1 which was examined, the curve-fitting functions used are

$$R_{bi} = f_1(I_b) = K_{bi} \cdot I_b \cdot e^{-H_{bi}\cdot I_b} + D_{bi} \tag{8}$$

$$R_{bi\_ib} = f_2(I_b) = K_{bi\_ib} \cdot e^{-H_{bi\_ib}\cdot I_b} + D_{bi\_ib} \tag{9}$$

$$R_{bi\_ic} = f_3(I_c) = K_{bi\_ic} \cdot e^{H_{bi\_ic}\cdot I_c} + D_{bi\_ic} \tag{10}$$

where K, H, D are constants which can be found by fitting to the measured data. For a particular device, only one of R_{bi_ib} and R_{bi_ic} is normally needed, depending on the device characteristics (see Section V, Part F). The Webster effect can be ignored as we stated previously. Other effects such as *emitter current crowding* and *lateral base widening* are very complex 3-D effects and their influences in the high current region strongly depends on the physical structure of the HBT. It would be difficult to obtain a unique analytical solution to account for these 3-D effects. Their influences on the HBT dc characteristics have been included in these nonlinear resistances in the new model. The Kirk effect was not observed in the region of interest for the HBT's tested here.

The combination of the new topology and appropriate nonlinear resistances present enormous flexibility to deal with the complexity in the high current region. This kind of set-up also yields a simple parameter extraction process.

In the new model the base current and collector current are two separate components which are controlled by the base-emitter voltage via two nonlinear resistances. The traditional relationship between I_b and I_c for a normal BJT via a constant current gain is replaced by a more complex implicit relationship. To support this, it has been observed that most AlGaAs/GaAs HBT's exhibit a region in the Gummel plot where $\log(I_c)$ and $\log(I_b)$ are straight lines. This implies that one can use an exponential function, which is always used to describe the I-V characteristics of a diode, to describe these two current components. On the other hand, as discussed in Section II, these two lines are not parallel as one would expect from a normal BJT. This fact renders the concept of a constant current gain β_F less meaningful, which is why some previous research has attempted to use a current-dependent β_F to describe the HBT

$$\beta_F \propto I_C^N \tag{11}$$

where N is a constant normally less than 1, and dependent on the process [1], [17], and [27]. Based on (1) and (2) given earlier, the factor N in [17] is found from the following expression:

$$N = 1 - \frac{n_{be\_ic}}{n_{be\_ib}}. \tag{12}$$

Since the BC junction is a homojunction, the reverse characteristics can be described by the same method as a normal homojunction BJT with a reverse current gain β_R. A current source I_{CC} used to simulate the collector current

$$I_{cc} = I_2 - \beta_R \cdot I_3. \tag{13}$$

The currents I_2 and I_3 are indicated in Fig. 3(a). For most HBT's β_R is very low and less than 0.01. This is because the reverse injection from base to emitter is suppressed by the BE heterojunction The voltage-controlled voltage source V_{be_ic} is used to transfer V_{be} to the diode D_{be_ic}, in order to generate the current I_c.

The model also includes several extrinsic elements: R_{bx}, R_e and R_c which are located outside the active intrinsic region of the HBT. R_{bx} is mainly base contact resistance. The base contact often presents the greatest problems for high frequency simulation [6], [8], and [18]. When the base contact is not a perfect ohmic contact, a Schottky diode might replace R_{bx} to describe the base contact. In the whole forward active region, this Schottky contact diode is forward biased and only presents a small resistance. In the reverse biased region, this diode can be modelled by a capacitance. It is worth indicating that the cut-off mode measurement, which is often used to extract parasitic parameters, may be inaccurate due to the existence of this contact capacitance. R_e is mainly the emitter contact resistance and will be discussed in detail in Section V. R_c is mainly a combination of collector contact resistance and collector bulk resistance.

The leakage currents often dominate the low-current region ($V_{be} < 1$ V in Fig. 2(a)). This can be easily modelled by adding a large resistance in parallel with each of the diodes D_{be_ib} and D_{be_ic}. These resistances are around 1 MΩ for the device used here. The value of these two resistances can be easily extracted from the curve obtained when Gummel-plot measurement results are plotted on a linear scale. The slopes of the I_b and I_c curves in the low current region indicate the values of these two resistances. Since our model is a large-signal model and normally works in the high current region, these resistances are ignored for simplicity.

B. Dynamic Part of the New HBT Model

The dynamic part of the model is simulated by several nonlinear capacitances. There are two junction capacitances in the HBT, C_{be}, and C_{bc}. C_{be} represents both the base-emitter junction depletion capacitance and the associated diffusion

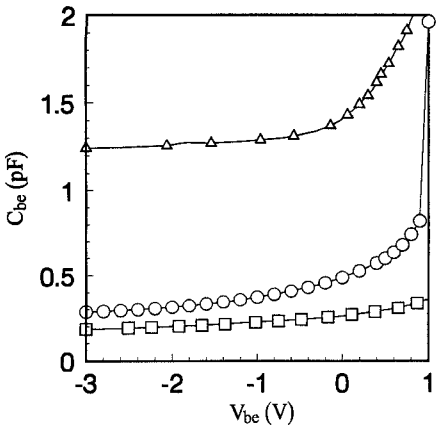

Fig. 4. Measured base-emitter capacitance (C_{be}) versus base-emitter voltage (V_{be}) for three different HBT's: Rockwell (triangles); Siemens (circles); TRW (squares).

capacitance. Although the base-emitter junction is a heterojunction, the depletion capacitance related to this junction can still be derived analytically using the depletion approximation [24], [25]. The formulas employed to describe this capacitance can be different so as to fit different processes. Fig. 4 shows several base-emitter junction capacitance measurement results. For most HBT's, the normal depletion capacitance formula can be used to describe this capacitance

$$C_J(V_j) = \frac{C_J(0)}{\left(1 - \frac{V_J}{\phi_J}\right)^m} \tag{14}$$

where V_J is the applied junction voltage, ϕ_J is the built-in potential, and m is the junction grading factor [5], [6], [8], and [9]. This formula is valid until V_J approaches ϕ_J. To avoid the singularity in (14) at the built-in potential voltage, we linearly extrapolate the CV curve after $V_J > F \cdot \phi_J$, where F is a factor between 0 and 1. This technique is used by SPICE and it does not accurately represent the depletion capacitance after $V_J > F \cdot \phi_J$. However, it is acceptable because the diffusion capacitance is dominant in this region [9].

In the regions of forward bias, (especially the region close or above the built-in potential ϕ_J) where the base-emitter junction is forward-biased and the base-collector junction is reverse-biased, mobile charges inside the HBT cause excess charge storage in different regions of the device. These excess charge-storage contributions correspond to extra components of capacitance. The four different charge components shown in Fig. 5 correspond to mobile minority charge, and these are related respectively to forward carrier injection in (i) the neutral emitter region (Q_1), (ii) the base-emitter SCR (Q_2), (iii) the neutral base region (Q_3), and (iv) the base-collector SCR (Q_4). These charge components can be evaluated by the following equation [8]:

$$Q_{DE} = Q_1 + Q_2 + Q_3 + Q_4 = \tau_E \cdot I_{CC} + \tau_{BE\_SCR} \cdot I_{CC} + \tau_B \cdot I_{CC} + \tau_{BC\_SCR} \cdot I_{CC} \tag{15}$$

where τ_E is the emitter base time constant (or emitter delay [8]), τ_{BE_SCR} is the emitter-base SCR transit time, τ_B is the base diffusion time and τ_{BC_SCR} is the base-collector SCR

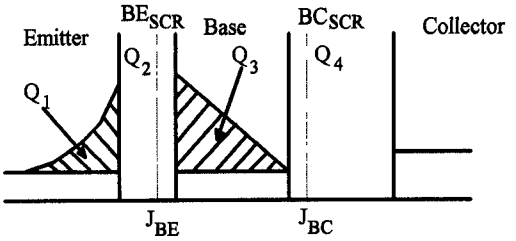

Fig. 5. Distribution of mobile minority charge components associated with the forward current.

transit time. This is a quite general formula and its validity does not depend on how the terms vary with bias conditions [8]. For a conventional Si BJT, τ_E and τ_B are the dominant terms in (15) and the Early effect and the Kirk effect can lead to a bias-dependent base diffusion time term. For the HBT case, τ_E and τ_B become less important compared to the base-collector SCR transit time [10], [22]. Since the width of the base-collector SCR and the velocity of the carriers in this region are the two main factors which determine τ_{BC_SCR}, (15) can be approximated by

$$Q_{DE} = \tau_F \cdot I_{CC} \tag{16}$$

with

$$\tau_F = \tau_0 + \frac{W^* \cdot \left(1 - \frac{V_{BC}}{\phi_{BC}}\right)^{M_{JBC}}}{\overline{\nu}_{BC\_SCR}} \tag{17}$$

where W^* is the width of base collector SCR, τ_0 is the delay term related to Q_1, Q_2 and Q_3, ϕ_{BC} and M_{JBC} are respectively the BC junction built-in potential and the junction grading factor, and $\overline{\nu}_{BC\_SCR}$ is the average velocity of a carrier in traversing the base-collector SCR region. For the HBT, the τ_0 term can be treated as a bias-independent term since HBT's normally have a very high base region doping level and the Early effect (base width modulation) is negligible. A value for $\overline{\nu}_{BC\_SCR}$ can be obtained from

$$\overline{\nu}_{BC\_SCR} = \frac{1}{W^*} \int_{SCR} \nu_{BC\_SCR}(x) \cdot dx. \tag{18}$$

Normally, it is a difficult task to obtain an accurate carrier velocity profile $\nu_{BC\_SCR}(x)$ in the base-collector SCR. There are several mechanisms which can be important in determining this velocity profile. With an increase in the carrier injection level, the electric field intensity in base-collector SCR decreases and this can maintain carriers in the Γ valley of the conduction band where carrier velocity is higher than other satellite valleys such as the L and X valleys. On the other hand, with an increase of V_{bc}, the electric field intensity increases. This can excite more carriers out of the Γ valley and can decrease the velocity of the carriers [2], [22]. Detailed information of the velocity profile could be obtained by using numerical analysis, but for the model presented here, a constant velocity is assumed as a good approximation.

Based on the above analysis, the individual charge terms in (15) are complex functions of bias conditions and can vary from device to device. The charge terms cannot be evaluated by direct measurement, but small-signal ac measurements may be used to reveal the diffusion capacitances which represent

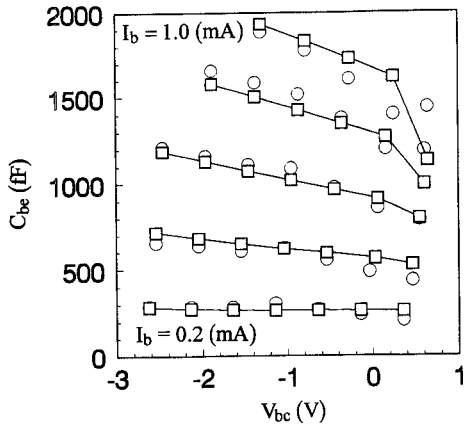

Fig. 6. Comparison of measured (circles) and modeled (solid lines and squares) diffusion capacitance as a function of collector current and base-collector voltage for the Siemens HBT #1.

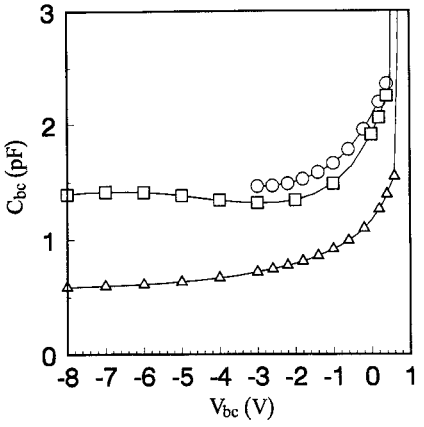

Fig. 7. Measured base-collector capacitance (C_{bc}) versus base-collector voltage (V_{bc}) for three different HBT's: Rockwell #1 (triangles); Siemens #2 (circles); Siemens #3 (squares).

the derivative of the charge terms with respect to their node voltages. Care must be taken in reconstructing charge formulas from measured capacitance data, since the charge conservation principle must hold if the charge term is not partitionable. As an example, Fig. 6 shows a C_{be} diffusion capacitance as a function of the bias condition. The solid lines represent the modelled results obtained from (16) and (17). Care must be taken to understand Fig. 6. Due to limitations of the set-up used constant conditions were used to compare the simulation with the measurement results. Due to the shape of the collector characteristics of the device used, the use of constant I_b resulted in a varying I_c.

Since several contrary mechanisms can compensate for each other, the assumption of τ_F as a bias-independent term for some devices and for parts of the forward active region (particularly those areas around a typical load line) might be a good approximation. For this case, the base-emitter capacitance could be represented by using the following formula which is similar to the equation given by Grossman and Choma [6]

$$C_{be\_\text{diffusion}} = C_{be0} \cdot \left(1 + \tanh\left(k \frac{V_{BE} - F \cdot V_J}{V_J}\right)\right). \quad (19)$$

It should be pointed out here that the "diode" element D_{be_ic} in the model of Fig. 3(a) does not represent a real semiconductor junction but acts instead as a nonlinear resistance used in the simulation of the behavior of the collector current. There is therefore no junction capacitance associated with this component.

The base-collector depletion capacitance is very important for HBT high frequency performance and it is normally reverse-biased in the HBT forward active region. Fig. 7 shows some C_{bc} measurement results for several different HBT's, which indicate that the capacitance normally can be modelled by the conventional formula (14). When this does not fit the measurement data, some alternative formulas can be obtained by curve-fitting. Further details on this important topic will be the subject of further work. When the HBT is reverse-biased, a similar method can be implemented to obtain the diffusion capacitance. The details are omitted here.

It is worth noting that this new model might be valid not only for the HBT, but also for modern BJTs, as they can exhibit similar departures from normal behavior such as non-uniform current gain and self-heating effects.

IV. Incorporating HBT Self-Heating Effects into Commercial Software Packages

The thermal conductivity of GaAs is significantly lower than that of Si. Since the self-heating effect is quite pronounced for most HBT's on a GaAs substrate, simulation of the junction temperature change and general thermo-electrical interaction is a basic requirement to ensure the accuracy of the HBT model. Unfortunately, most modern circuit simulators do not inherently simulate self-heating effects. A new method to simulate this effect within conventional circuit-oriented simulators is introduced here.

A. Self-Heating and its Effects on HBT Behavior

Whenever some electrical power is dissipated in a solid-state device, the temperature inside the device should increase correspondingly. This temperature increment invariably affects the device characteristics, which, in turn, can lead to an alteration in the dissipated power within the device. The whole process forms a thermo-electrical feedback loop. The feedback can be positive or negative for different operating conditions. One familiar example is thermal runaway in BJT's, where a positive feedback loop leads to an uncontrolled increase in the junction temperature.

Since HBT's can carry high current with very high current density in a small emitter area, and bearing in mind the low thermal conductivity of the GaAs substrate, HBT's can experience severe local heating. This has several direct consequences, as shown in Fig. 2(b). The first one is that the HBT output characteristics often show a negative slope in the high current region, which might be expected to cause stability problems at low frequencies. A second consequence is that the current gain is severely compressed in the high current region. In Fig. 2(b), the current gain decreases about 30 percent when V_{ce} increases from 1.5–6 volts. A third result is gain collapse in the very high power region of operation which can only be observed in multi-finger power HBT's [19]. These phenomena

related to self-heating make the task of device modelling more difficult than usual.

B. Electrical Analog Equivalent Circuit of Thermal Flow in the HBT

The temperature distribution across the HBT at a fixed dc bias point can be obtained by solving the heat flow problem analytically or numerically, in two- or three-dimensions. Generally speaking, the temperature distribution across the HBT is not uniform, even for different points on the same emitter finger. Gain collapse can only be adequately modelled by accounting for this non-uniform temperature distribution. As a first order approximation, one can assume that the temperature across the HBT is a constant. Based on this assumption, the HBT's temperature can be expressed as a function of the dc dissipated power

$$T_J = f(P_D) \tag{20}$$

where T_J is the computation junction temperature and P_D is the dc dissipated power. This can be further approximated as

$$T_J = T_0 + R_{TH} \cdot P_D \tag{21}$$

where R_{TH} is the computation thermal resistance and T_0 is the ambient temperature. This equation is only suitable for the dc situation, when an ac signal is added to the device, a more general form of this equation must be used to simulate the computation junction temperature and the computation thermal resistance must be replaced by a computation thermal impedance

$$Z_{TH} = \sum_{n=1}^{m} \frac{R_{TH}^{(n)}}{1 + j\omega R_{TH}^{(n)} \cdot C_{TH}^{(n)}}. \tag{22}$$

The computation thermal impedance can be approximated by a multi-section RC network which presents several different thermal time constants [20]. These time constants normally vary from microseconds to minutes as they correspond to different self-heating mechanisms. The first self-heating mechanism is local heating and the temperature rise is confined within an area which is less than about ten times the area of the base-collector SCR [6], [26]. This kind of temperature rise has a very short time constant and is difficult to eliminate by packaging and heat-sinking [6]. The second self-heating mechanism is the heat flow from the heat source to the heat-sink and has quite a long time constant. Equation (22) is only an approximation of the real self-heating effects, but it does provide an easy way to incorporate the self-heating effect in commercial simulators. The thermal coupling between the different devices in the same MMIC chip can also be modelled by a similar method.

C. Using a Temperature-Sensitivity Partitioning Technique to Incorporate Self-heating Effects Within Circuit Simulators

Most modern circuit simulators do not include a direct way to simulate the self-heating effect even though nearly all of them include active device models with temperature dependences included internally. Before the user starts the simulator, a constant temperature must be assigned to the system and the simulator assumes that devices retain this temperature throughout the whole simulation process. This kind of program structure cannot predict the self-heating effect since it needs to know the temperature of the device *a priori*.

One direct way to solve this problem is to introduce one extra temperature parameter to each of the active device model parameters and to each passive (e.g. MMIC) circuit element. The instantaneous temperature of the circuit can be calculated from a thermal analogue electrical equivalent circuit. An iterative loop can solve the temperature of the devices and the circuit variables together by combining the electrical and thermal equivalent circuits and using normal CAD solution techniques. In this direct form, such a method could be unattractive to most modern circuit designers, since a very large increase in CPU time would be involved. For instance, the SPICE BJT model has forty parameters. Letting every one of them become a temperature-dependent parameter means that we introduce forty nonlinear control functions to replace the original forty constant parameters. Linear elements would be changed to nonlinear elements, leading to a substantial computational overhead in commercial simulators.

To address this issue we introduce a novel technique here called the *temperature-sensitivity partitioning technique*. It is a compromise between simulating the circuit without any self-heating and performing a more complete computationally-intensive self-heating analysis. The core of this technique is to partition the circuit elements and modelling parameters into two categories: temperature-sensitive parameters and temperature-insensitive parameters. Some parameters such as the saturation current of a PN junction should be in the temperature-sensitive group while the resistance of a contact could be in the temperature-insensitive group. The physical basis of this technique is very clear. After partitioning, the temperature-sensitive parameters and devices are changed to temperature-dependent elements and devices. An extra node is added for each of them. Then the general circuit iteration loop is used to solve all the circuit variables and the temperature together. Since normally only several temperature-sensitive parameters are critical for self-heating effects, the numerical effort reduces to a minimum compared to the more general, unrestricted case. Using this technique to simulate HBT self-heating, we choose the saturation currents and the ideality factors of the D_{be_ib} and D_{be_ic} as temperature sensitive parameters (see (1)–(4)). Another junction diode D_{bc} in the model might also be sensitive to the junction temperature, but we leave it in the temperature-insensitive group for simplicity. A way of implementing (1)–(4) within the framework of the HP-MDS simulator, is described in [23]. We leave all other model parameters in the temperature-insensitive group.

This method has been successfully implemented in several CAD environments, and very good results have been obtained.

V. The Parameter Extraction Procedure

The end-user of a model must also know how to extract the parameters of that model correctly. In general, there are two basic approaches available to do this. Firstly, through the use of advanced optimization techniques, the model parameters can be adjusted to fit the measurement results. When a good fit has been achieved for all measurements over all operating

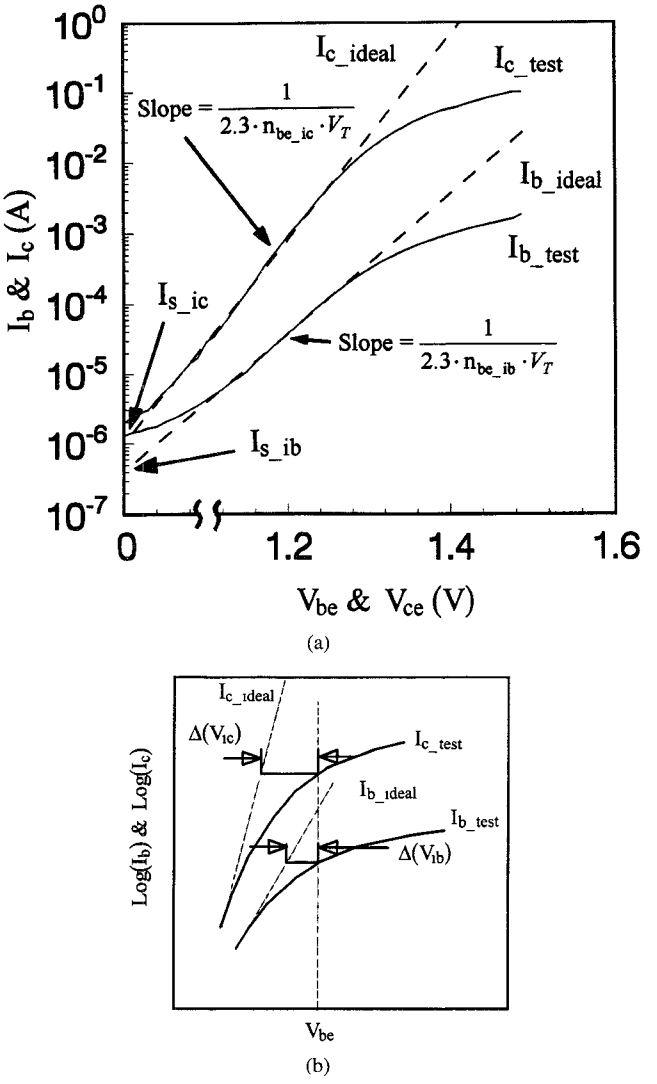

Fig. 8. (a) Graphical extraction of HBT dc model parameters from the Gummel plot; (b) graphical extraction of two base nonlinear resistances from high current region of the Gummel plot.

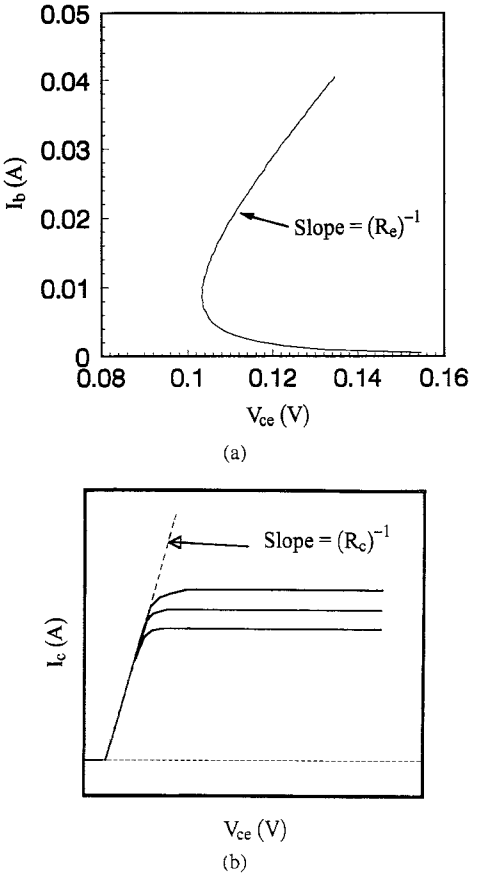

Fig. 9. (a) Graphical determination of the emitter resistance from open-collector measurement result; (b) graphical extraction of the HBT collector resistance from output characteristics.

conditions of interest, the result is a set of parameters which can be used by circuit designers. Recently, several software packages based on this approach have become widely used. The main problem associated with this method is that a physically-unrealistic solution can occur due to the presence of many local-minimum solutions. The other approach is based on performing a specially-designed group of sequential measurements, accompanied by direct extraction of model parameters by suitable processing of these results [8]. In the authors' opinion, the model parameter extraction process is as important as the model itself, and the best way to perform parameter extraction is through a combination of the above two methods, aiming at a reduction to a minimum of the number of optimization variables involved, thereby avoiding the multi-solution problem and also saving on computation effort.

Since the proposed model is basically formed by the exponential functions, which are widely used to describe I-V characteristics of semiconductor junctions, and resistance accompanied by the new topology shown in Fig. 3(a), the parameter extraction process becomes very simple. The steps are as follows:

1) Perform the necessary forward and reverse measurements to obtain the Gummel-Plots. This measurement can be performed with $V_{bc} = 0$ (forward) and $V_{be} = 0$ (reverse).
2) From the forward Gummel-plot, the two straight lines on the log-linear plot in the medium-current region give $I_{s\_ib}, I_{s\_ic}, n_{be\_ib}$ and n_{be_ic} directly by graphical methods as shown in Fig. 8(a).
3) From the reverse Gummel-Plot, I_{s_bc} and n_{bc} can be extracted by a similar method.
4) The emitter resistance is determined by using the open-collector method [8]. This is performed by measuring the saturation voltage V_{CES} for different base currents while keeping the collector current zero. By plotting V_{ce} versus I_b. the slope of the curve can be used to determine emitter resistance. An application of this method in the case of an HBT is illustrated in Fig. 9(a).
5) The collector resistance can be obtained by directly observing the slope of the collector output characteristics as shown in Fig. 9(b). This measurement poses similar problems to that of R_e. in that R_c is defined as a bulk resistance for the collector region plus the collector contact resistance. This bulk resistance may be modulated by the collector current, but it is believed here that a simplified linear resistance is sufficient to simulate the

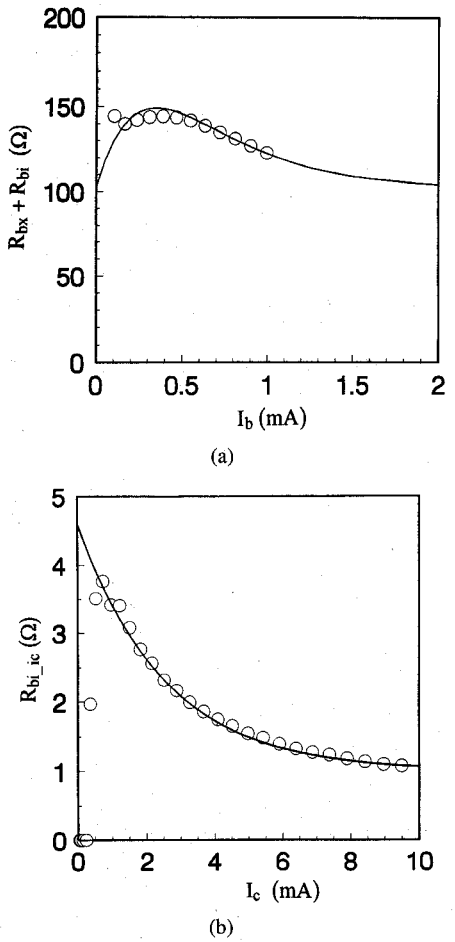

Fig. 10. (a) Comparison of the measured (circles) and modeled (solid lines) $R_{bx} + R_{bi}$ as a function of base current for the Siemens HBT #1; (b) comparison of the measured (circles) and modeled (solid lines) R_{bi_ic} as a function of the collector current for the Siemens HBT #1.

HBT under large-signal conditions. Problems may still arise when the HBT is in the saturation region, but this area is normally avoided by circuit designers, and the difficulty should then be minimized.

6) Turning our attention now to the high current region of the Gummel plot of Fig. 8(b), and the deviation of the measured curves from the ideal straight lines predicted by the exponential equation discussed earlier.

For a given base-emitter voltage, the deviations from the ideal lines are not necessarily equal, i.e., we find that $\Delta(V_{ib}) \neq \Delta(V_{ic})$. This inequality is accounted for in this model by a distributed base resistance network as shown in Fig. 3. Performing a dc circuit analysis of this network yields the following expressions:

$$\Delta(V_{ib}) = n_{be\_ib} \cdot V_T \ln\left(\frac{I_{b\_\text{ideal}}}{I_{b\_\text{test}}}\right) = (R_{bx} + R_{bi} + R_{bi\_ib}) \cdot I_{b\_\text{test}} + R_e \cdot I_{e\_\text{test}} \tag{23}$$

$$\Delta(V_{ic}) = n_{be\_ic} \cdot V_T \ln\left(\frac{I_{c\_\text{ideal}}}{I_{c\_\text{test}}}\right) = (R_{bx} + R_{bi} + R_{bi\_ic}) \cdot I_{b\_\text{test}} + R_e \cdot I_{e\_\text{test}}. \tag{24}$$

TABLE I
PARAMETER VALUES FOR SIEMENS HBT #1

Symbol	Value	Symbol	Value
R_{bx} (Ohm)	0.0	A_{n_ic} $1/C^o$	$5.0\ 10^{-4}$
R_c (Ohm)	2.0	B_{n_ic} $1/(C^o)^2$	0.0
R_e (Ohm)	24.0	T_{s_ic} (K)	1800
R_{th} (C/W)	600	I_{s_bc} (A)	$3.70596\ 10^{-22}$
C_{jbc} (fF)	24	n_{bc}	2.6249
ϕ_{jbc} (Volt)	1.4	K_{bi} (Ohm)/(mA)	0.36
M_{jbc}	0.6	H_{bi} 1/(mA)	3.6
C_{jbe} (fF)	20	D_{bi} (Ohm)	0.7
ϕ_{jbc} (Volt)	1.3	K_{bi_ib} (Ohm)/(mA)	0.0
M_{jbc}	0.5	H_{bi_ib} 1/(mA)	0.0
I_{s_ib} (A)	$8.12014\ 10^{-18}$	D_{bi_ib} (Ohm)	0.0
n_{bc_ib}	1.65651	K_{bi_ic} (Ohm)	2.9
A_{n_ib} $1/C^o$	$5.0\ 10^{-4}$	H_{bi_ic} 1/(mA)	370
B_{n_ib} $1/(C^o)^2$	0.0	D_{bi_ic} (Ohm)	102
T_{s_ib} (K)	1800		
I_{s_ic} (A)	$2.82186\ 10^{-22}$		
n_{bc_ic}	1.186389		

Two distinct cases are possible here

1) $\Delta(V_{ib}) < \Delta(V_{ic})$

Here the nonlinear resistance R_{bi_ic} is used to compensate for this difference, and R_{bi_ib} is set to zero. The values of $R_{bx} + R_{bi}$ and R_{bi_ic} are extracted by using the following expressions:

$$R_{bx} + R_{bi} = \frac{\Delta(V_{ib}) - R_e \cdot I_{e\_\text{test}}}{I_{b\_\text{test}}} \tag{25}$$

$$R_{bi\_ic} = \frac{\Delta(V_{ic}) - \Delta(V_{ib})}{I_{c\_\text{test}}}. \tag{26}$$

2) $\Delta(V_{ib}) > \Delta(V_{ic})$

Now, R_{bi_ic} is set to zero, and R_{bi_ib} is used for compensation. In this case, $R_{bx} + R_{bi}$ and R_{bi_ib} are extracted using the following expressions:

$$R_{bx} + R_{bi} = \frac{\Delta(V_{ic}) - R_e \cdot I_{e\_\text{test}}}{I_{b\_\text{test}}} \tag{27}$$

$$R_{bi\_ib} = \frac{\Delta(V_{ib}) - \Delta(V_{ic})}{I_{b\_\text{test}}}. \tag{28}$$

From the above expressions, R_{bi_ic} (or R_{bi_ib}) and $R_{bx} + R_{bi}$ can be extracted from the Gummel-Plot measurement,

but there is no clear method to separate R_{bx} and R_{bi} by dc measurement only. Normally these resistances are nonlinear functions of the base and collector currents, but since R_{bx} is dominated by the contact resistance, we can constrain it to a constant value. The nonlinear part of the function is then described by R_{bi}.

In essence, we now have described the base resistance by a four element network where one value is constant (R_{bx}), one value is zero (R_{bi_ib} or R_{bi_ic}) and the remaining two (R_{bi} and R_{bi_ic} or R_{bi_ib}) are nonlinear functions. These functions are strongly dependent on the base and collector currents because they are modulated by the carrier concentration in the intrinsic base region. The value of R_{bi} normally increases with decreasing base current, and, in the low current region numerical errors often dominate the extraction results. These phenomena conspire to create quite large errors in the low current region. These do not significantly degrade the accuracy of the model, however, since the current level is very low and the voltage drop across the resistance is extremely small. For the midcurrent region, these resistances are dependent on the base current and show sharp variation. For the high current region, the resistances tend to a constant value. The extraction results of $R_{bx} + R_{bi}$ and R_{bi_ic} for a Siemens HBT are shown in Fig. 10(a) and (b).

7) The *computation thermal resistance* can be determined after extraction of all the other dc parameters. The thermal resistance value is adjusted to make the output characteristics of the simulation fit the measured characteristics and to obtain the same negative slope in the high current region. At this stage only the thermal resistance is adjustable, so a unique solution can be obtained very easily. The other thermal parameters related with the two temperature-dependent diodes can be obtained by measuring Gummel-Plots at different temperatures [6], [13]. The thermal capacitance is not so important for high frequency applications due to the fact that the thermal reaction time constant is very large compared to the microwave variations, so the junction temperature remains relatively constant for fast periodic variations. The thermal capacitor typically has a value of several microfarads.
8) The base charge component Q_b can be extracted after extraction of all the dc and thermal parameters. At this stage, all the dc parameters are fixed and the model can give a good prediction of the dc characteristics. Broadband small-signal S parameters of the device are then measured at numerous bias points in the forward bias plane to form a net or grid which covers the entire desired region of operation. The density of this grid depends on the desired accuracy and on acceptable measurement times: the more bias points, the higher accuracy. The two capacitances of the model can then be optimized to make all four S parameters fit the measurement results at every bias point, giving the two capacitance data tables as functions of the bias applied. Since only two variables are involved in this optimization process, a unique solution can be achieved relatively easily. After $C_{be}(V_{be}, V_{ce})$ and $C_{bc}(V_{be}, V_{ce})$ have been obtained, the data is curve-fitted to (14) (16), and (17) to obtain the corresponding coefficients. This procedure can guarantee that the following integral is path-independent

$$Q_b = \int_0^{V_{be}} C_{be}(\xi, 0)\, d\xi + \int_0^{V_{bc}} C_{bc}(V_{be}, \eta)\, d\eta \quad (29)$$

where Q_b is a function of the bias point, and η and ξ are dummy variables. For the simplest case, the charge can be assumed to be partitionable and represented as $C_{be}(V_{be})$ and $C_{bc}(V_{bc})$. Equations (14) and (19) can be used to curve-fit the measurement results. It is worth noting here that the capacitance model strongly depends on the HBT physical structure and may differ in form from device to device.

The above process should always guarantee reasonable capacitance values for the whole active region. After these results are available, an analytical function can always be obtained to model the dynamic part of the HBT model. Fig. 6 shows comparison of the modelling and simulation results of C_{be} for a Siemens HBT.

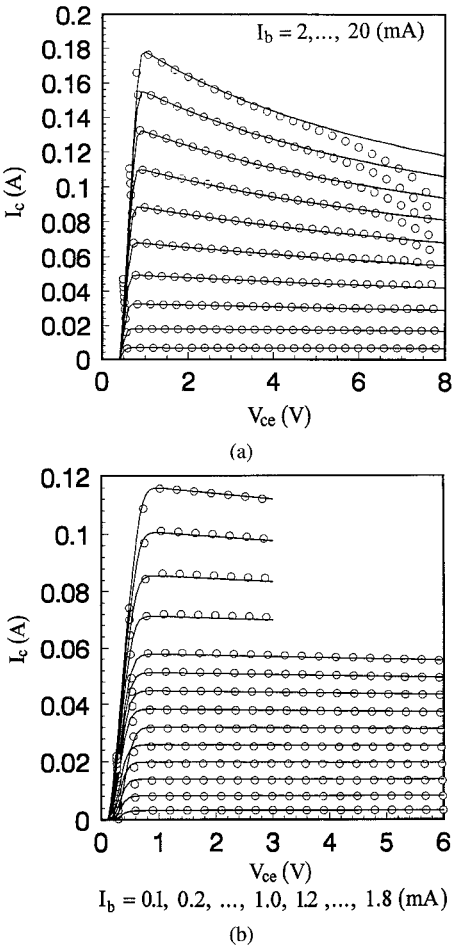

Fig. 11. Comparison of the measured (circles) and simulated (solid lines) output characteristics for (a) Siemens HBT #2; (b) Rockwell HBT #1.

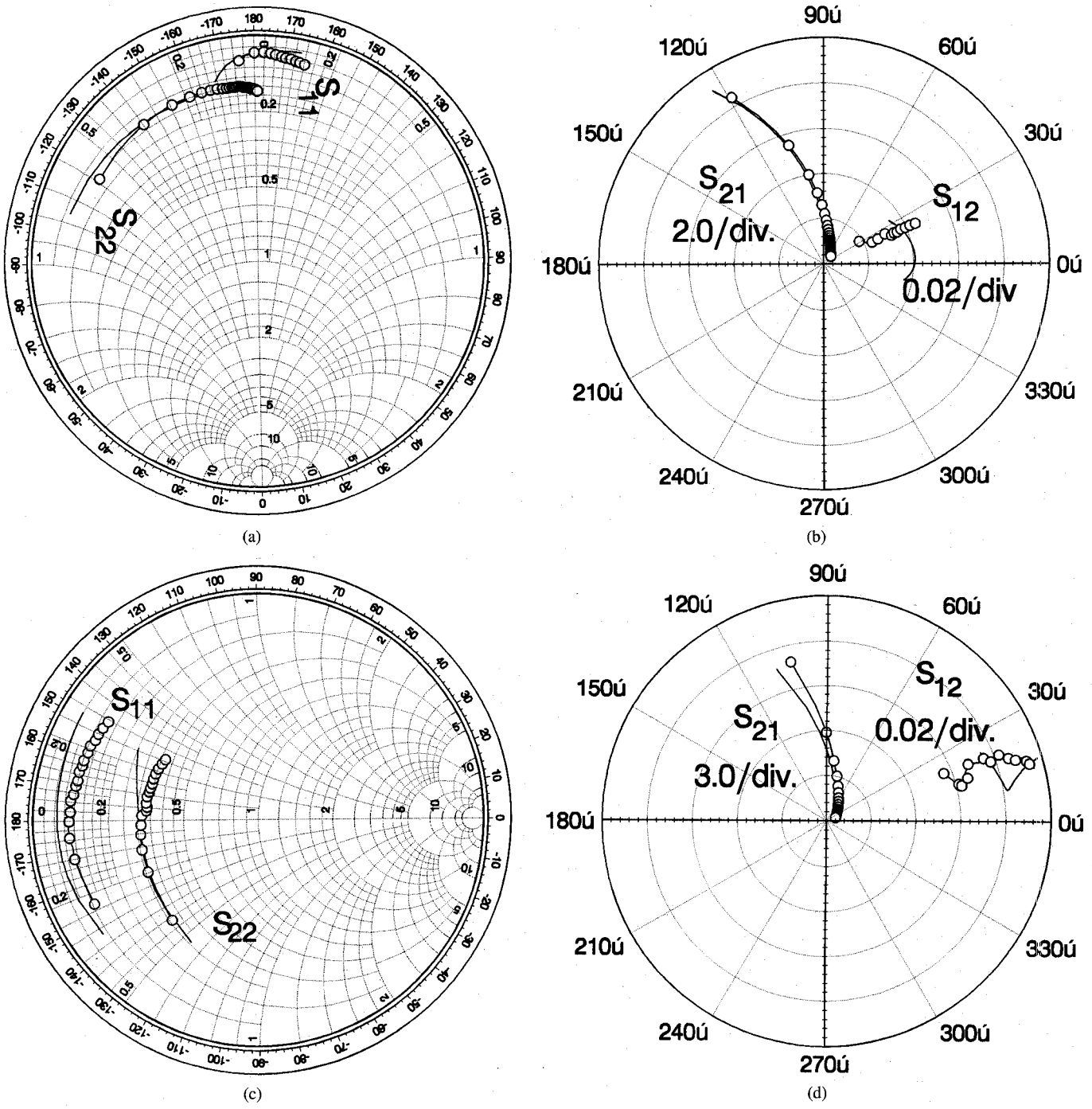

Fig. 12. Comparison of the measured (solid lines and circles) and simulated (solid lines) S parameters for (a) S_{11} and S_{22} for Siemens HBT #2; Freq. = 0.5–12.0 GHz, I_c = 78.5 (mA), V_{ce} = 3 (V) ; (b) S_{12} and S_{21} for Siemens HBT #2; Freq. = 0.5–12.0 GHz, I_c = 78.5 (mA), V_{ce} = 3 (V); (c) S_{11} and S_{22} for Rockwell HBT #1; Freq = 0.57–9.8 GHz, I_c = 55 (mA), V_{ce} = 3 (V); (d) S_{12} and S_{21} for Rockwell HBT #1; Freq = 0.57–9.8 GHz, I_c = 55 (mA), V_{ce} = 3 (V).

In this way, the whole parameter set can be extracted using the above step-by-step process by performing dc and broadband (CW) small-signal S parameters measurements, plus some simple curve-fitting. This gives us a quasi-static model where time delay is included in the base charge model.

VI. Verification of the New HBT Model

The full parameter extraction process has been carried out for several AlGaAs/GaAs HBT's obtained from Siemens AG, Germany, and Rockwell International, USA, and the parameter values for Siemens HBT #1 are listed in Table I. Before the small-signal measurement was carried out, a dummy structure was measured to enable dc-embedding of the probe pads [21]. Model verification is separated into three parts: dc, broadband small-signal S parameters and large-signal power sweep measurement. The parameters of the model are fixed for all three situations so the results are consistent. The simulation results reported are obtained from HP-MDS, however the

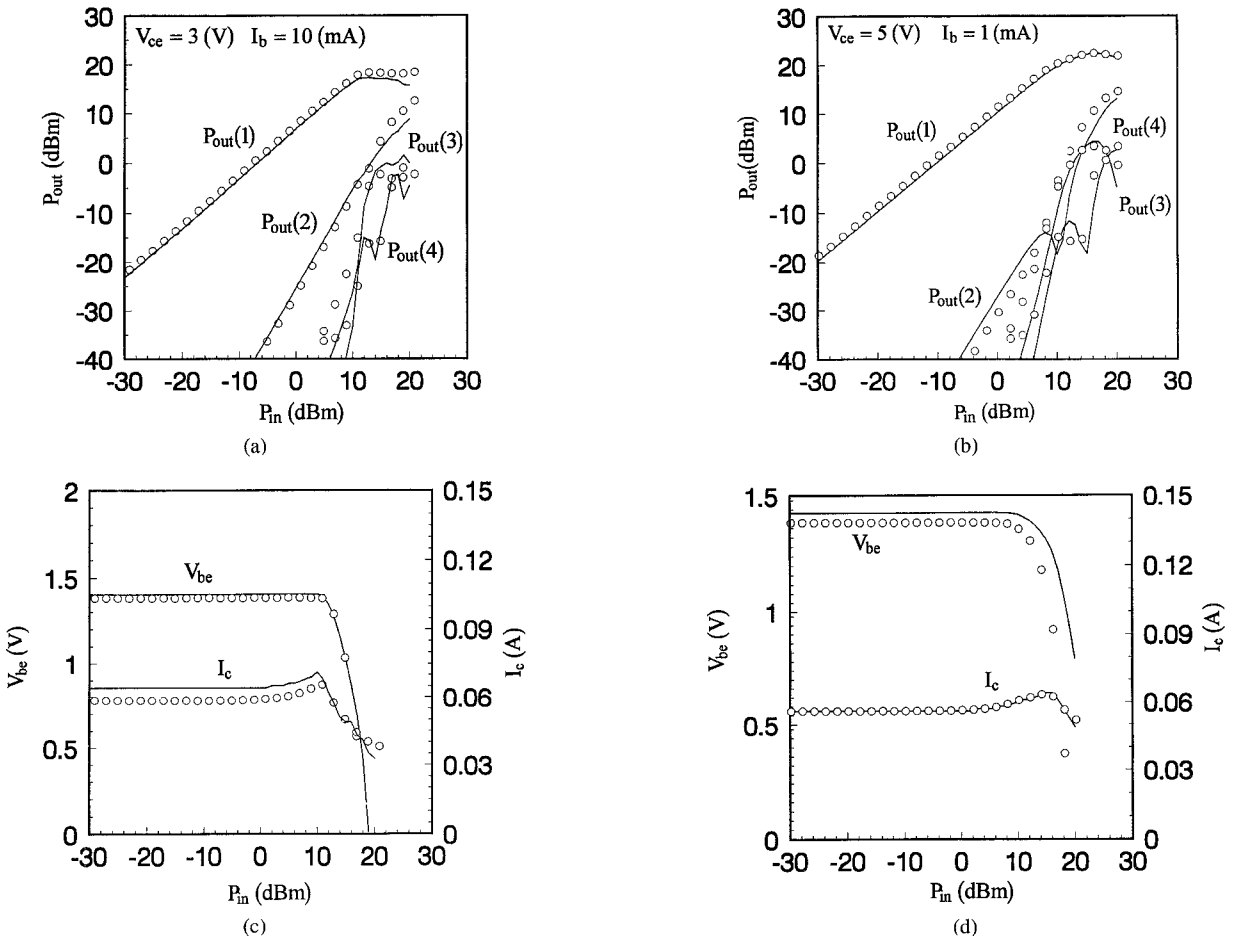

Fig. 13. Comparison of the measured (circles) and simulated (solid lines) 2 GHz power-sweep results for (a) Siemens HBT #2; (b) Rockwell HBT #1; measured (circles), and simulated (solid lines) associated bias point shift for (c) Siemens HBT #2; (d) Rockwell HBT #1.

model has also been implemented in HARMONICA from Super-Compact and can also be added to SPICE.

For the dc situation, the parameters used for the simulation were extracted by the above method. The results show very good agreement with the measurement results (Fig. 11(a) for Siemens HBT #2 and Fig. 11(b) for Rockwell HBT). The discrepancy shown between measured and modelled data in the high V_{ce} region (Fig. 11(a)) is due to gain collapse. Since this effect is caused by the nonunifrom temperature distribution across the emitter fingers of multi-finger HBT's, it can not be modelled by the present model which assumes a uniform temperature distribution across the device.

For the same parameters and models, HP MDS was used to generate the small-signal S parameters, and these are compared with the measurement results in Fig. 12(a)–(d) and show good agreement at all bias points.

The final and most important step to verify the model is through the use of a power sweep measurement. In this arrangement, the device is tested in a 50-Ω amplifier environment, and the output fundamental and harmonic power levels are recorded as the input power is swept from small-signal through to sufficiently large values to produce significant gain compression. Since all the model parameters were extracted from dc and broad band S parameter measurements, the power sweep is an independent verification method for validation of the model. The measurement and simulation results give excellent agreement as shown in Fig. 13(a) and (b). It must be emphasized that no post-adjustment of the large-signal model was made to improve the fit in any of the data comparisons shown.

VII. Conclusion

A new HBT large-signal model has been developed which includes self-heating effects. The proposed model is based on experimental observation and physical analysis which leads to a very direct parameter extraction process. The introduction of a new topology to split the base into several regions allows the base and collector currents to be tracked very accurately. A thermal sub-circuit which includes a simplified *computational thermal resistance* and *computational thermal capacitance*, is employed to simulate self-heating effects. A new *temperature-sensitivity partitioning technique* is introduced to incorporate self-heating effects within general commercially-available software. Finally, this model is intended to be of practical utility, and, indeed, can be readily incorporated within the usual microwave software environments such as HP-MDS, LIBRA and HARMONICA, or even SPICE.

ACKNOWLEDGMENT

The authors would like to acknowledge the device samples and assistance received from Siemens AG, Munich Germany and Rockwell International, Thousand Oaks, CA. The authors also wish to thank Dr. J. A. Higgins for helpful discussions and support.

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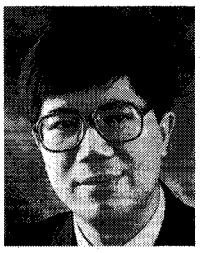

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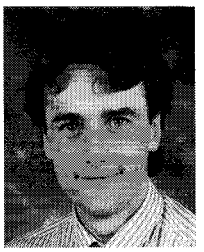

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Thomas J. Brazil (M'87) was born in Co. Offaly, Ireland, in 1952. He received the B.E. degree in electrical engineering from University College Dublin in 1973, and was awarded the Ph.D. degree in 1977 by the National University of Ireland.

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